REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance width NOR 5962-R064-93. - drw	93-01-11	Michael A. Frye
B	Update drawing to current requirements. Editorial changes throughout. – drw	02-09-04	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV																			
SHEET																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Gary Zahn

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
89-8-8

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, CMOS, MICROPROCESSOR COMPATIBLE, DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88765**

SHEET 1 OF 12

DSCC FORM 2233
APR 97

5962-E535-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88765	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Relative accuracy
01	7549S	Dual, CMOS, 12-bit DAC	±1.0 LSB
02	7549T	Dual, CMOS, 12-bit DAC	±0.5 LSB

1.2.2 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to DGND	-0.3 V dc to +17 V dc
V_{REFA}, V_{REFB} to AGND	±25 V dc
V_{RFBA}, V_{RFBB} to AGND	±25 V dc
Digital input to DGND	-0.3 V dc to V_{DD}
V_{PIN15}, V_{PIN17} to DGND	-0.3 V dc to V_{DD}
AGND to DGND	-0.3 V dc to V_{DD}
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	+450 mW 1/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	+120°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+14.25 V dc to +15.75 V dc
A-reference voltage (V_{REFA})	+10 V dc
B-reference voltage (V_{REFB})	+10 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Derate above T_A = +75°C at +6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	Guaranteed minimum resolution	1, 2, 3	All	12		Bits
Relative accuracy	RA		1, 2, 3	01		±1.0	LSB
			1	02		±1.0	
			2, 3, 12			±0.5	
Differential nonlinearity	DNL	Guaranteed monotonic to 12-bits	1, 2, 3	All		±1.0	LSB
Gain error 3/	A_E		1, 2, 3	01		±6.0	LSB
			1	02		±6.0	
			2, 3, 12			±3.0	
Supply rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5.0%, full scale outputs	1	All		±0.01	%/%
			2, 3			±0.02	
Output leakage current	I_{OUTA}	DAC A loaded with all 0's	1	All		20	nA
			2, 3			250	
	I_{OUTB}	DAC B loaded with all 0's	1	All		20	nA
			2, 3			250	
Output current settling time to 0.01% of FSR 4/	t_{SL}	I_{OUT} load = 100Ω, C_{EXT} = 13 pF, DAC output measured from falling edge of WR	4	All		1.5	µs
Feedthrough error, V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB} 4/ 5/	FT	$V_{REFA} = V_{REFB}$ = ±20 Vpp, 10 kHz sine wave, DAC register loaded with all 0's	4	All		-65	dB
Reference input resistance	R_{IN}		1, 2, 3	All	7.0	18	kΩ
Reference input resistance match (V_{REFA}/V_{REFB})	R_{MIN}		1, 2, 3	01		±3.0	%
			1	02		±3.0	
			2, 3, 12			±2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input high voltage	V_{IH}		1, 2, 3	All	2.4		V
Digital input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$	1	All		±1.0	µA
			2, 3			±10	
Input capacitance 4/	C_{IN}		4	All		7.0	pF
Analog output capacitance 4/	C_{OUTA}	DAC A = all 0's	4	All		80	pF
		DAC A = all 1's				160	
Analog output capacitance 4/	C_{OUTB}	DAC B = all 0's	4	All		80	pF
		DAC B = all 1's				160	
Functional test		See 4.3.1c	7, 8	All			
Address valid to write setup time	t_{AWS}	See figure 3	9	All	50		ns
			10, 11		110		
Address valid to write hold time	t_{AWH}	See figure 3	9, 10, 11	All	0		ns
Data setup time	t_{DS}	See figure 3	9	All	180		ns
			10, 11		240		
Data hold time	t_{DH}	See figure 3	9, 10, 11	All	5		ns
Chip select or update to write setup time	t_{CWS}	See figure 3	9, 10, 11	All	20		ns
Chip select or update to write hold time	t_{CWH}	See figure 3	9, 10, 11	All	0		ns
Write pulse width	t_{WR}	See figure 3	9	All	170		ns
			10, 11		250		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clear pulse width	t_{CLR}	See figure 3	9	All	170		ns
			10, 11		250		
Supply current	I_{DD}		1, 2, 3	All		5.0	mA

1/ $V_{REFA} = V_{REFB} = +10$ V, $V_{PIN15} = V_{PIN16} = V_{PIN17} = 0$ V unless other wise specified. All tests are guaranteed over a supply voltage range of $V_{DD} = 15$ V ±5.0%, however, all measurements are made at $V_{DD} = +15$ V unless other wise specified.

2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

3/ Measured using internal feedback resistor and includes effects of leakage current and gain temperature coefficient.

4/ Subgroup 4 (t_{SL}, FT, C_{IN}, C_{OUTA} and C_{OUTB} measurements) shall be measured only for the initial test and after process or design changes which may affect these tests.

5/ Feedthrough can be further reduced by connecting the metal lid to ground.

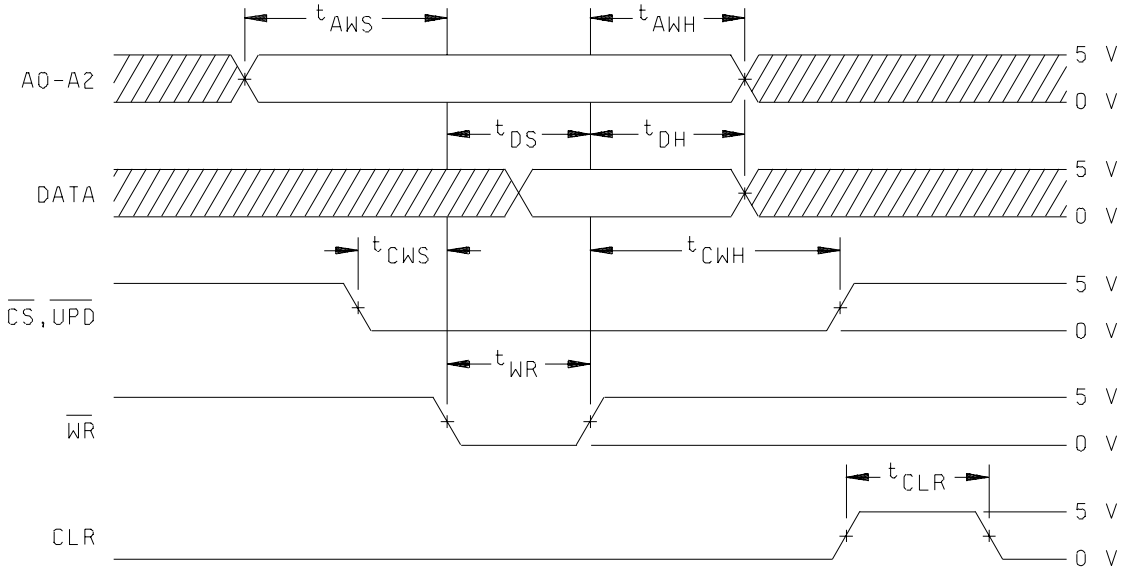
Device types	All
Case outline	R
Terminal number	Terminal symbol
1	DB3
2	DB2
3	DB1
4	DB0
5	$\overline{UPD}$
6	A2
7	A1
8	A0
9	$\overline{CS}$
10	$\overline{WR}$
11	CLR
12	DGND
13	V_{REFB}
14	R_{FBB}
15	I_{OUTB}
16	AGND
17	I_{OUTA}
18	R_{FBA}
19	V_{REFA}
20	V_{DD}

FIGURE 1. Terminal connections.

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	Function
0	X	X	1	X	X	X	No data transfer
0	1	1	X	X	X	X	No data transfer
1	X	X	X	X	X	X	All register cleared
0	1	0	⌐⌐	0	0	0	DAC A low nibble register loaded from data bus
0	1	0	⌐⌐	0	0	1	DAC A mid nibble register loaded from data bus
0	1	0	⌐⌐	0	1	0	DAC A high nibble register loaded from data bus
0	1	0	⌐⌐	0	1	1	DAC A register loaded from input registers
0	1	0	⌐⌐	1	0	0	DAC B low nibble register loaded from data bus
0	1	0	⌐⌐	1	0	1	DAC B mid nibble register loaded from data bus
0	1	0	⌐⌐	1	1	0	DAC B high nibble register loaded from data bus
0	1	0	⌐⌐	1	1	1	DAC B register loaded from input registers
0	0	1	⌐⌐	X	X	X	DAC A, DAC B registers updated simultaneously from input registers

0 = Logic low level
1 = Logic high level
X = Don't care

FIGURE 2. Truth table.



Notes:
1. All input signal rise and fall times are measured from 10% to 90% of +5.0 V, $t_r = t_f = 20$ ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

FIGURE 3. Timing diagram.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 12
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10***, 11***, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** See 4.3.1e.
*** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

d. Subgroup 12 test is used for grading and part selection at T_A = +25°C and is not included in PDA calculations.

e. Subgroup 4 (t_{SL}, FT, C_{IN}, C_{OUTA} and C_{OUTB} measurements) shall be measured only for the initial test and after process or design changes which may affect these capacitance measurements.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-09-04

Approved sources of supply for SMD 5962-88765 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8876501RA	24355	AD7549SQ/883B
5962-8876502RA	24355	AD7549TQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Bay F-1 Raheen Ind. Estate Limerick, Ireland